Fig.1

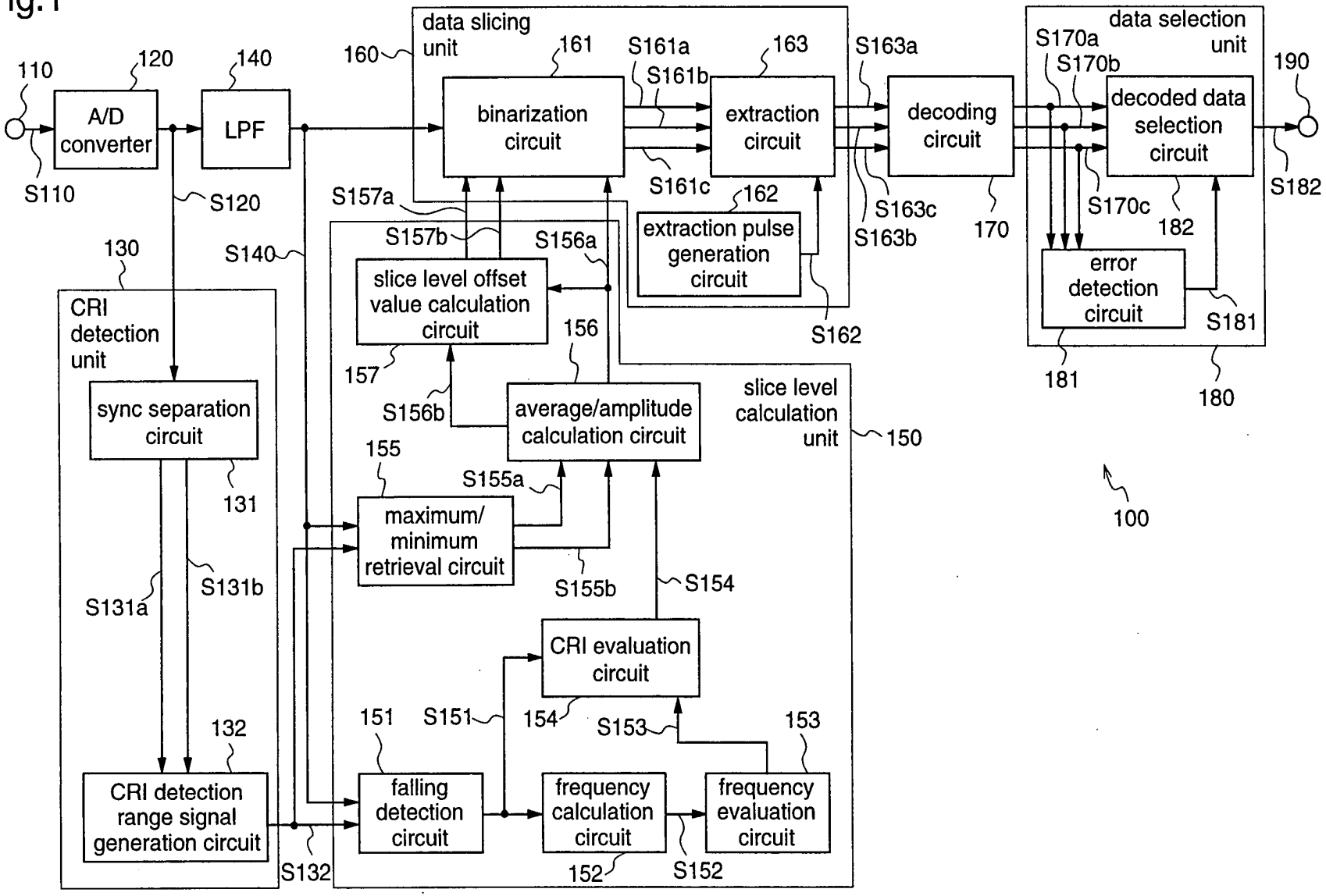
110
120
140
160
data slicing unit
161
S161a
S161b
163
S163a
data selection unit
S170a
S170b
190
A/D converter
LPF
binarization circuit
extraction circuit
decoding circuit
decoded data selection circuit
S110
S120
S161c
S163c
S163b
170
S170c
182
S182
S157a
162
extraction pulse generation circuit
S157b
S156a
S140
130
slice level offset value calculation circuit
error detection circuit
S181
CRI detection unit
156
S162
157
181
180
sync separation circuit
S156b
average/amplitude calculation circuit
slice level calculation unit
150
155
S155a
131
maximum/ minimum retrieval circuit
100
S131a
S131b
S155b
S154
CRI evaluation circuit
132
151
S151
154
S153
153
CRI detection range signal generation circuit
falling detection circuit
frequency calculation circuit
frequency evaluation circuit
S132
152
S152

Fig.2

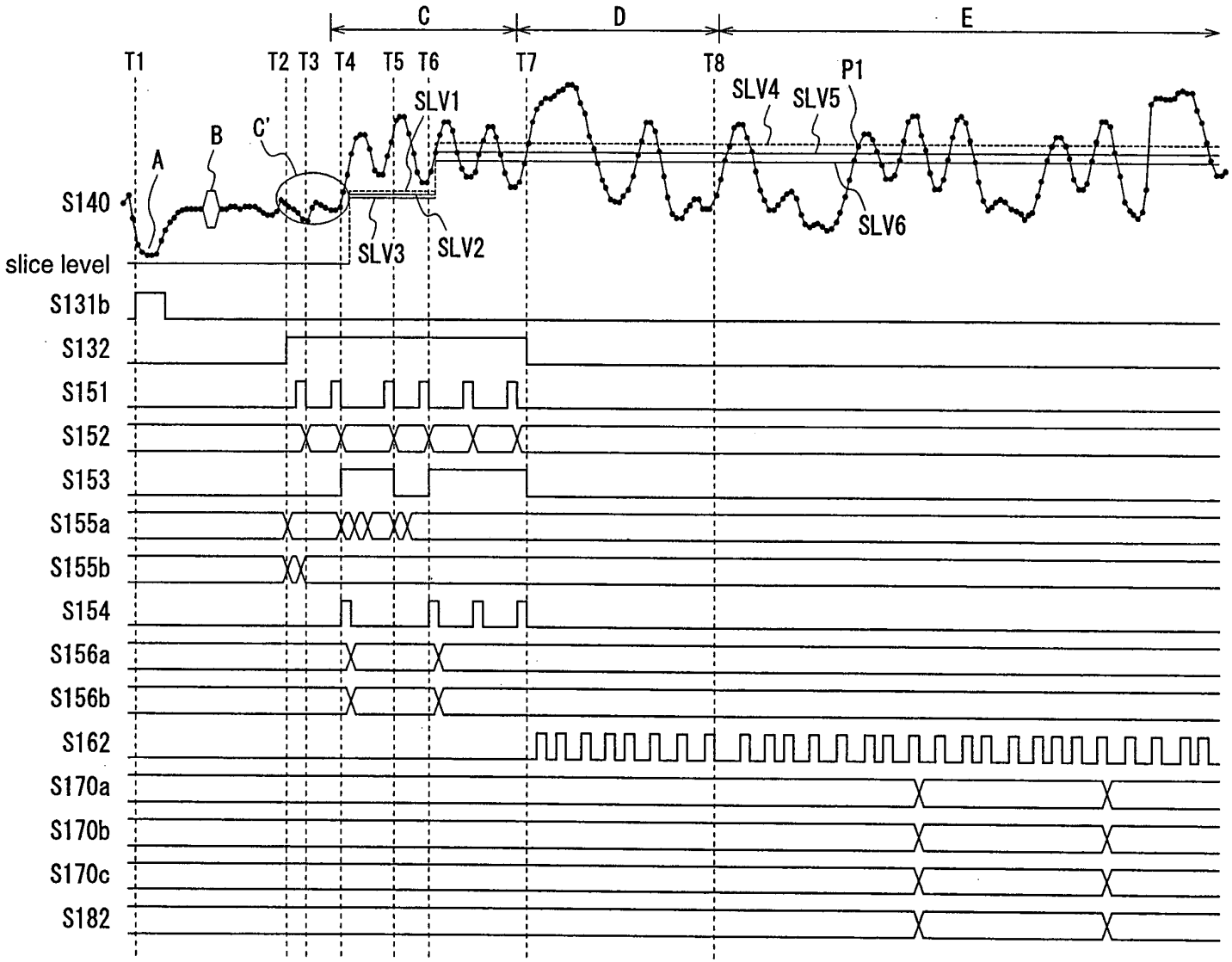
C
D
E
T1
T2
T3
T4
T5
T6
T7
T8
A
B
C'
SLV1
SLV2
SLV3
SLV4
SLV5
SLV6
P1
S140
slice level
S131b
S132
S151
S152
S153
S155a
S155b
S154
S156a
S156b
S162
S170a
S170b
S170c
S182

Fig.3

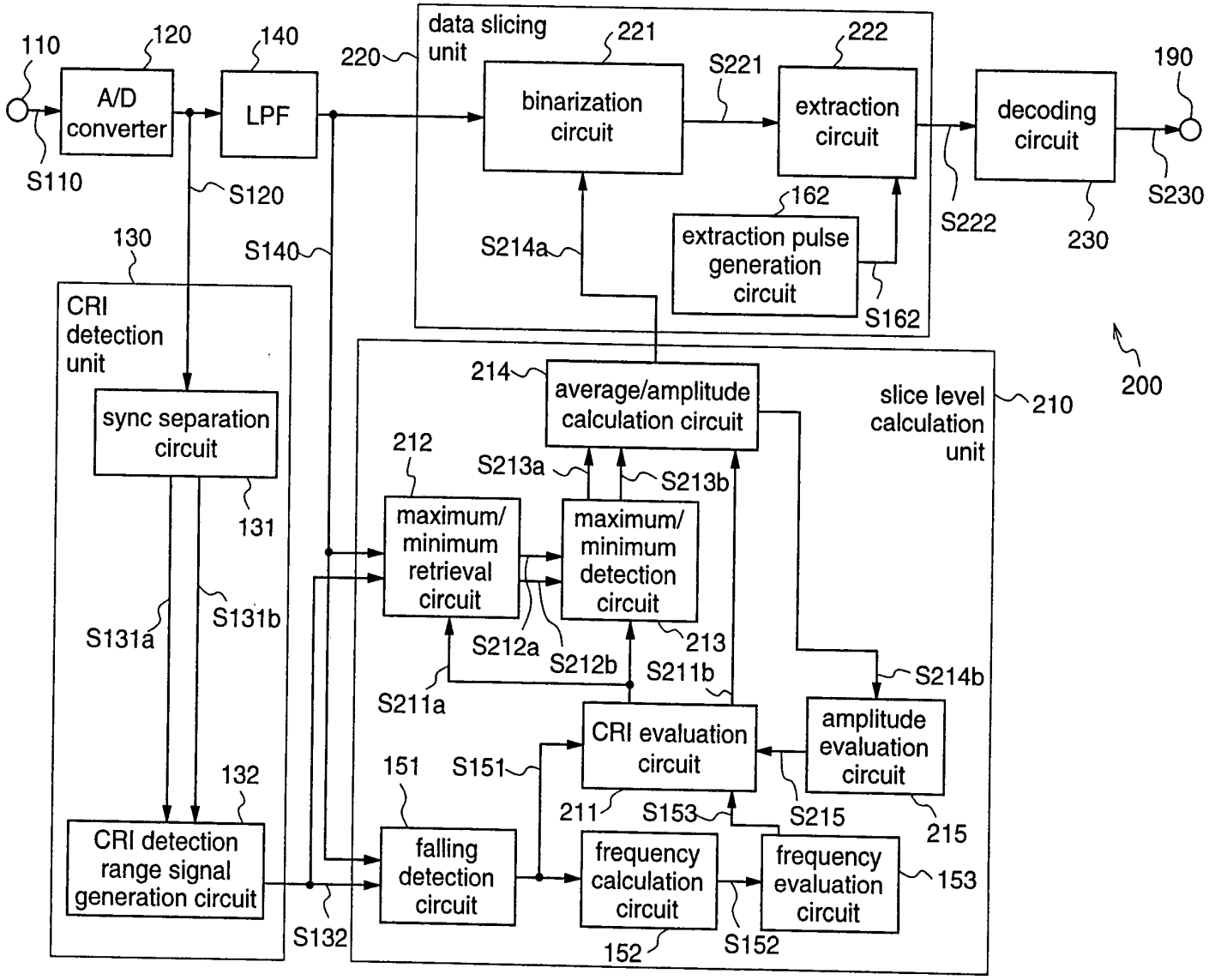
110
120
140
220
data slicing unit
221
222
190
A/D converter
LPF
binarization circuit
S221
extraction circuit
decoding circuit
S110
S120
S222
230
S230
162
extraction pulse generation circuit
S214a
S140
S162
130
200
CRI detection unit
214
average/amplitude calculation circuit
slice level calculation unit
210
sync separation circuit
212
S213a
S213b
maximum/ minimum retrieval circuit
maximum/ minimum detection circuit
131
S131a
S131b
S212a
S212b
213
S211b
S214b
S211a
CRI evaluation circuit
amplitude evaluation circuit
151
S151
132
211
S153
S215
215
CRI detection range signal generation circuit
falling detection circuit
frequency calculation circuit
frequency evaluation circuit
153
S132
152
S152

Fig.4

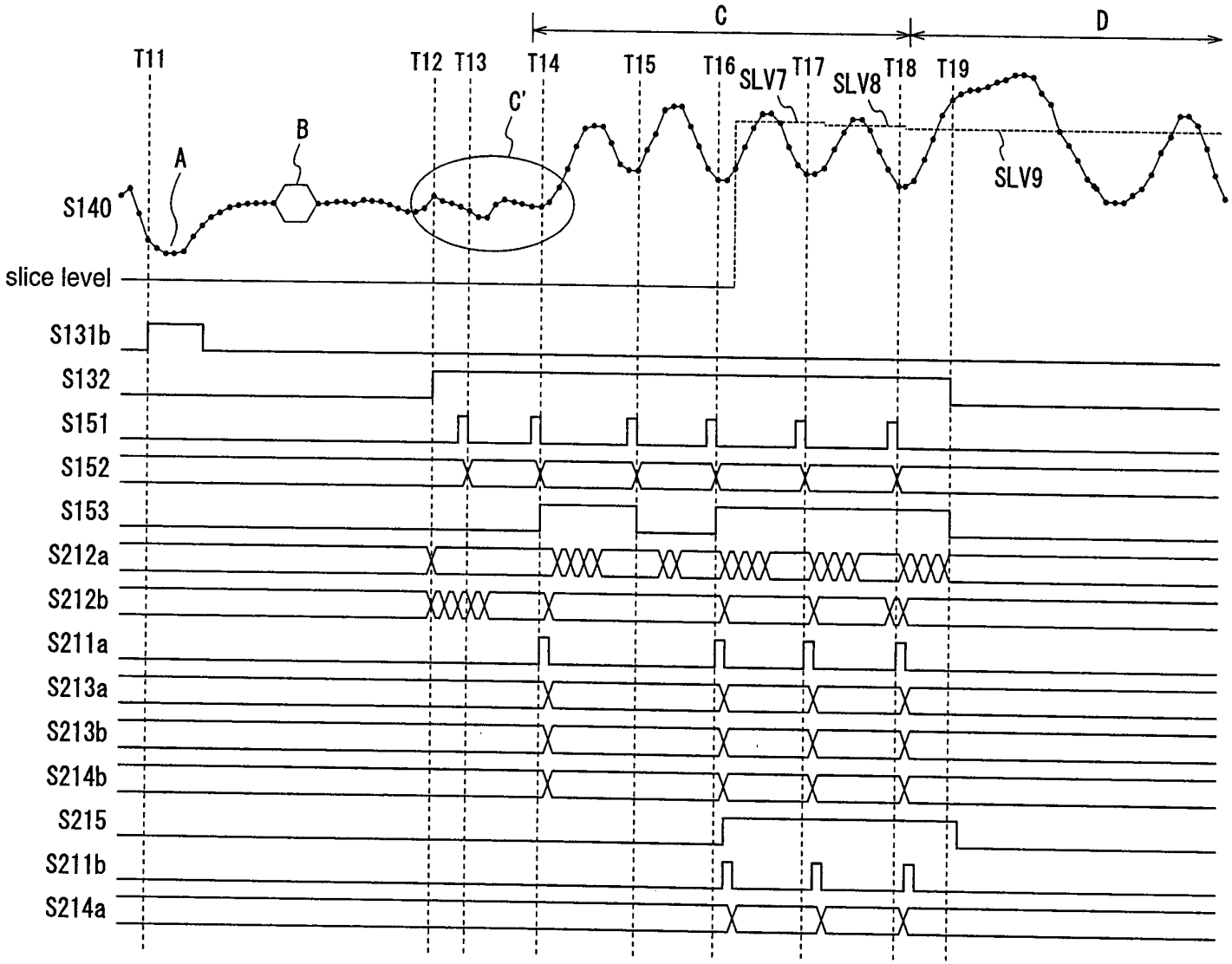
C
D
T11
T12
T13
T14
T15
T16
SLV7
T17
SLV8
T18
T19
A
B
C'
SLV9
S140
slice level
S131b
S132
S151
S152
S153
S212a
S212b
S211a
S213a
S213b
S214b
S215
S211b
S214a

Fig.5

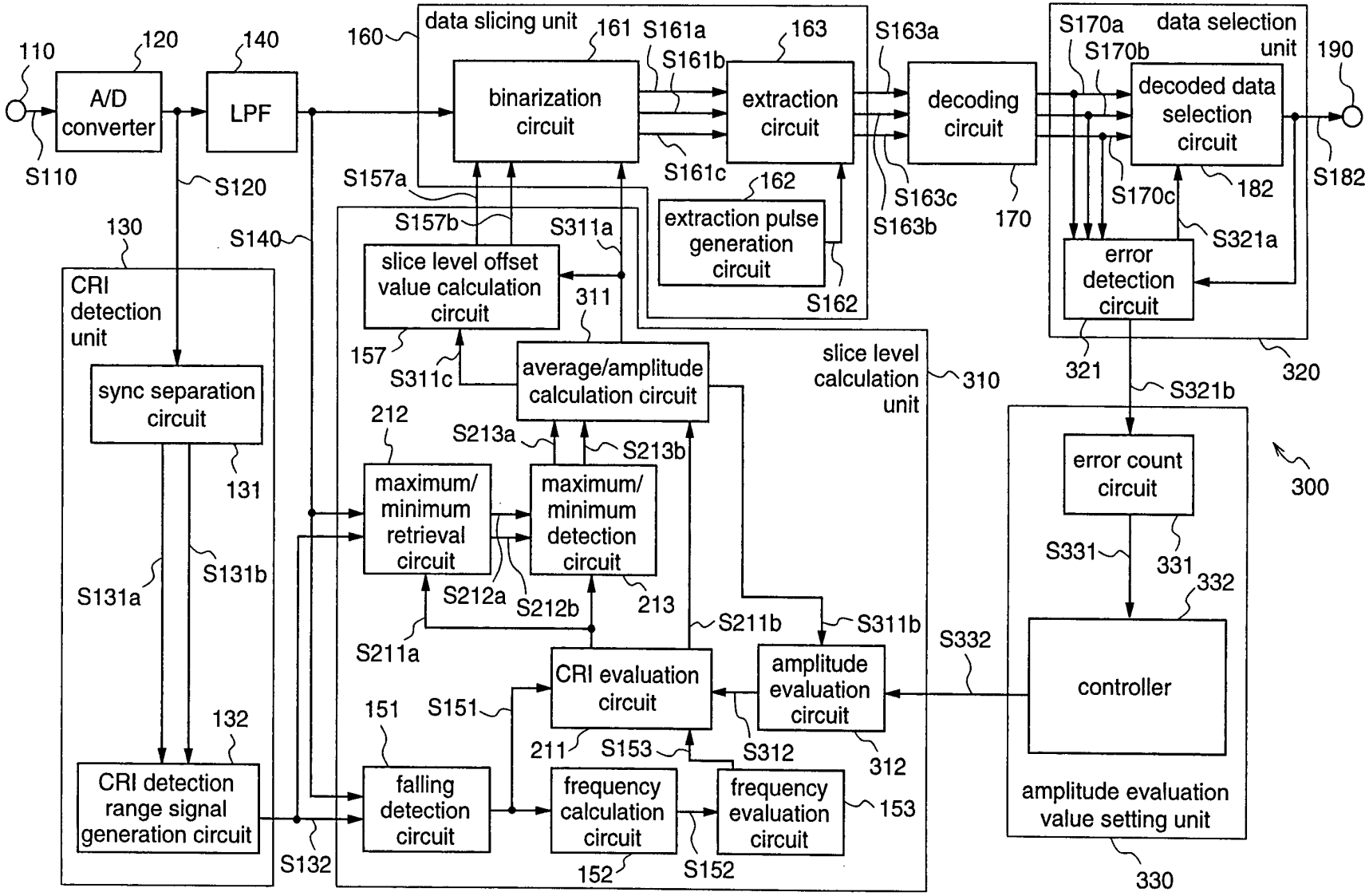
110
A/D converter
120
LPF
140
S110
S120
160
data slicing unit
161
S161a
S161b
S161c
binarization circuit
163
extraction circuit
162
extraction pulse generation circuit
S162
S163a
S163b
S163c
decoding circuit
170
S170a
S170b
data selection unit
190
decoded data selection circuit
182
S182
S170c
S321a
error detection circuit
321
320
S321b
S157a
S157b
S311a
slice level offset value calculation circuit
311
157
S311c
average/amplitude calculation circuit
slice level calculation unit
310
130
CRI detection unit
S140
sync separation circuit
131
S131a
S131b
132
CRI detection range signal generation circuit
S132
212
S213a
S213b
maximum/ minimum retrieval circuit
maximum/ minimum detection circuit
S212a
S212b
213
S211a
S211b
S311b
151
S151
falling detection circuit
CRI evaluation circuit
211
S153
frequency calculation circuit
152
S152
frequency evaluation circuit
153
S312
amplitude evaluation circuit
312
S332
controller
amplitude evaluation value setting unit
330
error count circuit
S331
331
332
300

Fig.6

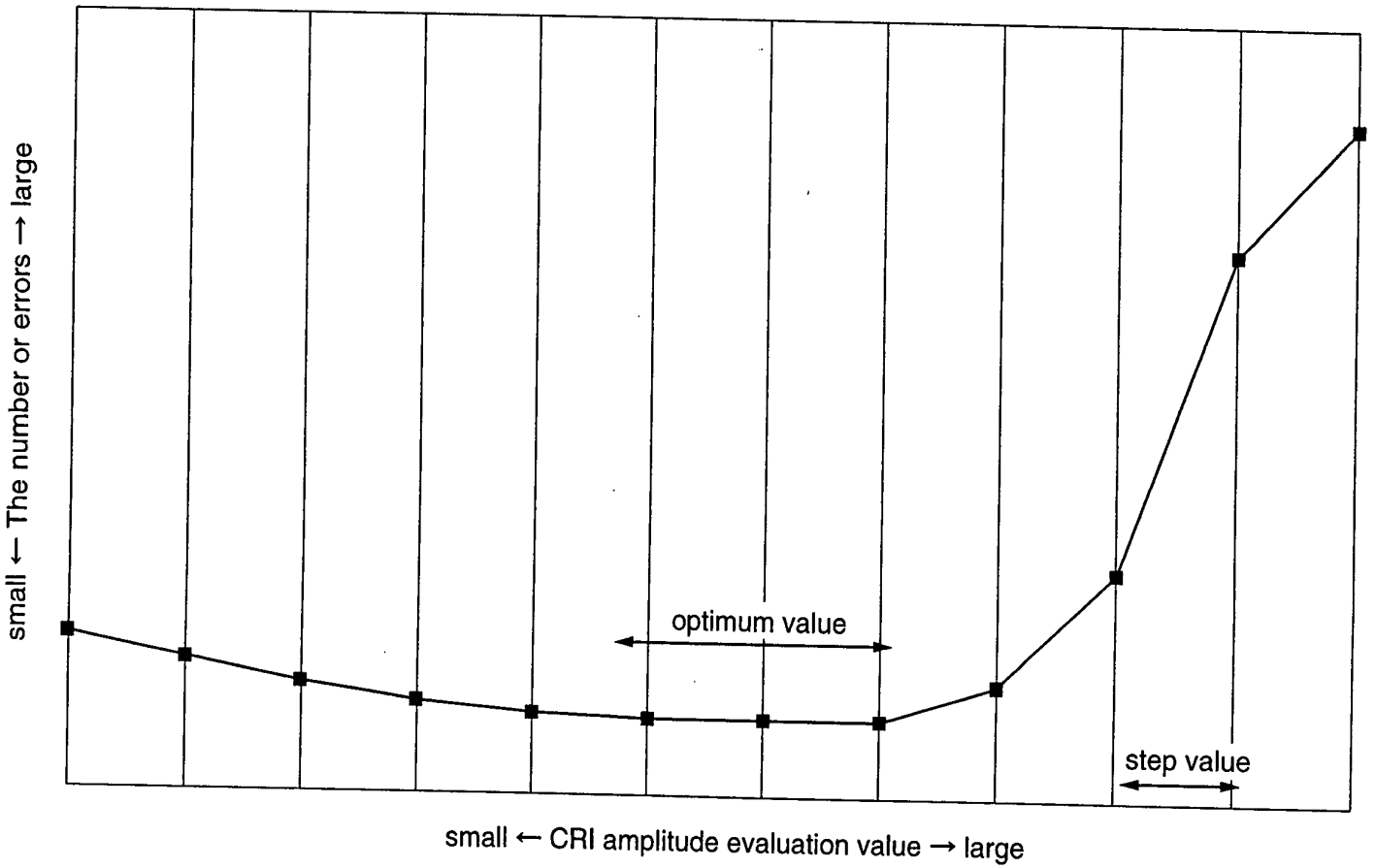
small ← The number or errors → large
optimum value
step value
small ← CRI amplitude evaluation value → large

Fig.7

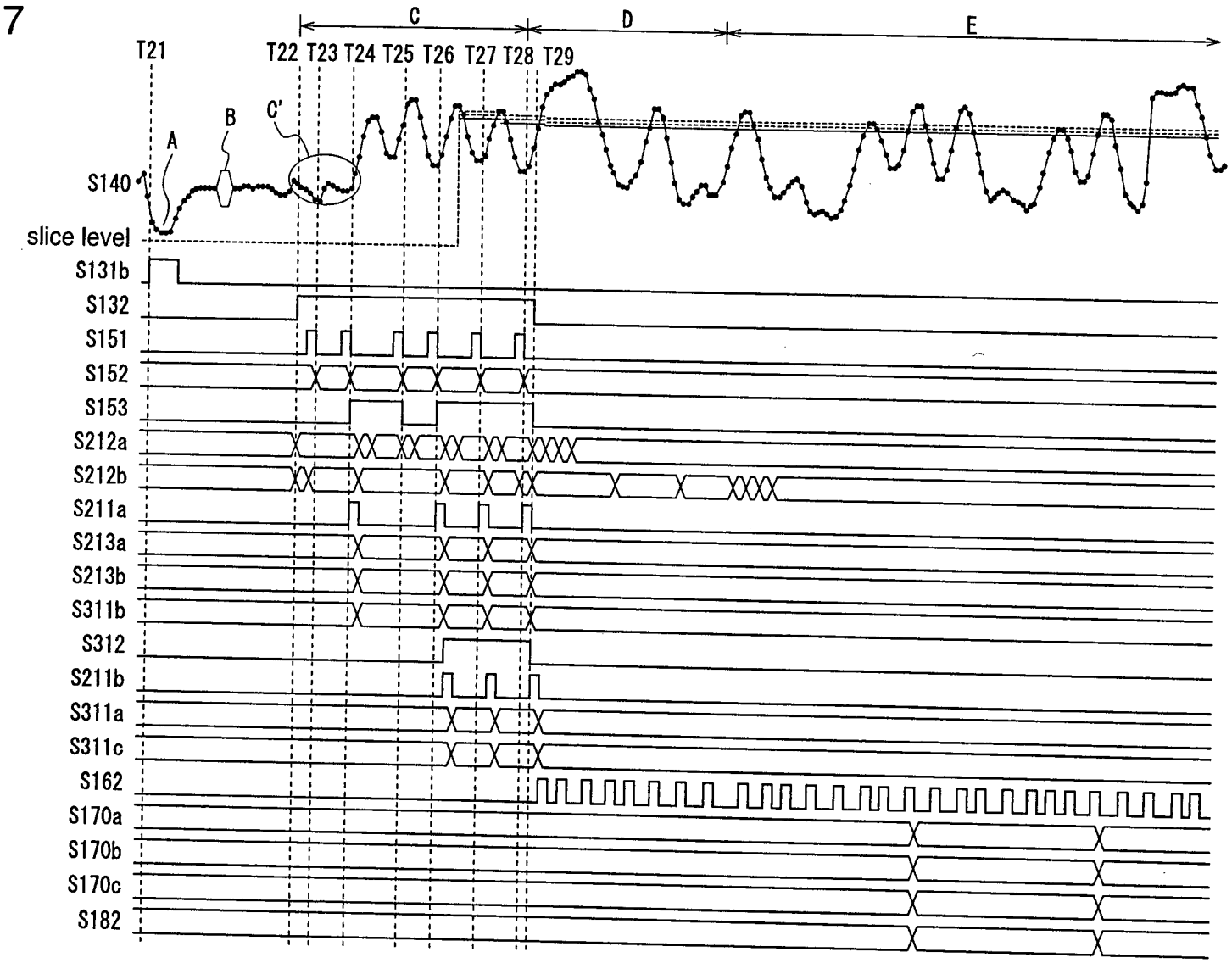
C
D
E
T21
T22 T23 T24 T25 T26 T27 T28 T29
A
B
C'
S140
slice level
S131b
S132
S151
S152
S153
S212a
S212b
S211a
S213a
S213b
S311b
S312
S211b
S311a
S311c
S162
S170a
S170b
S170c
S182

Fig.8

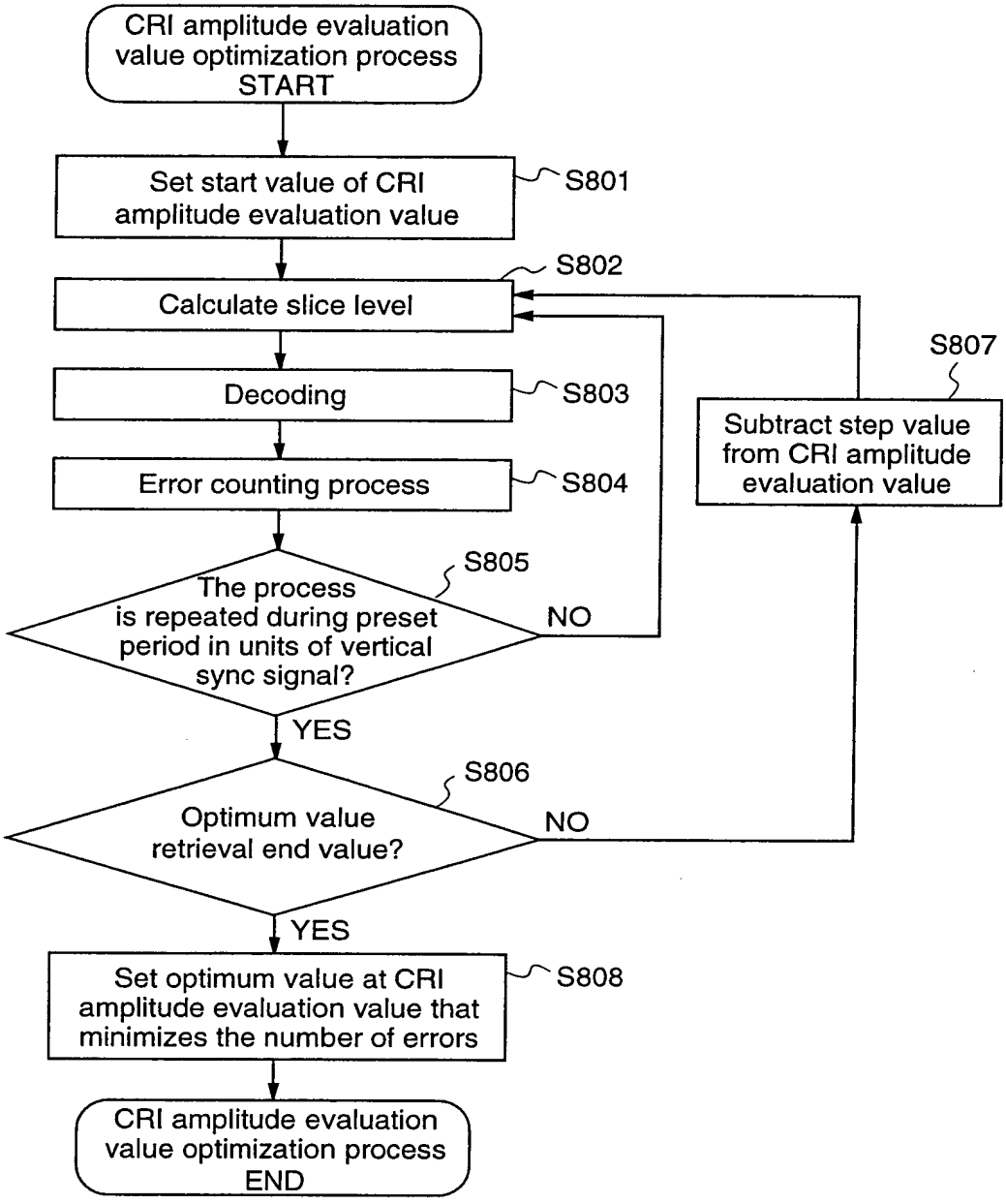
CRI amplitude evaluation value optimization process START
Set start value of CRI amplitude evaluation value
S801
Calculate slice level
S802
Decoding
S803
Error counting process
S804
The process is repeated during preset period in units of vertical sync signal?
S805
NO
YES
Optimum value retrieval end value?
S806
NO
YES
Subtract step value from CRI amplitude evaluation value
S807
Set optimum value at CRI amplitude evaluation value that minimizes the number of errors
S808
CRI amplitude evaluation value optimization process END

Fig.9

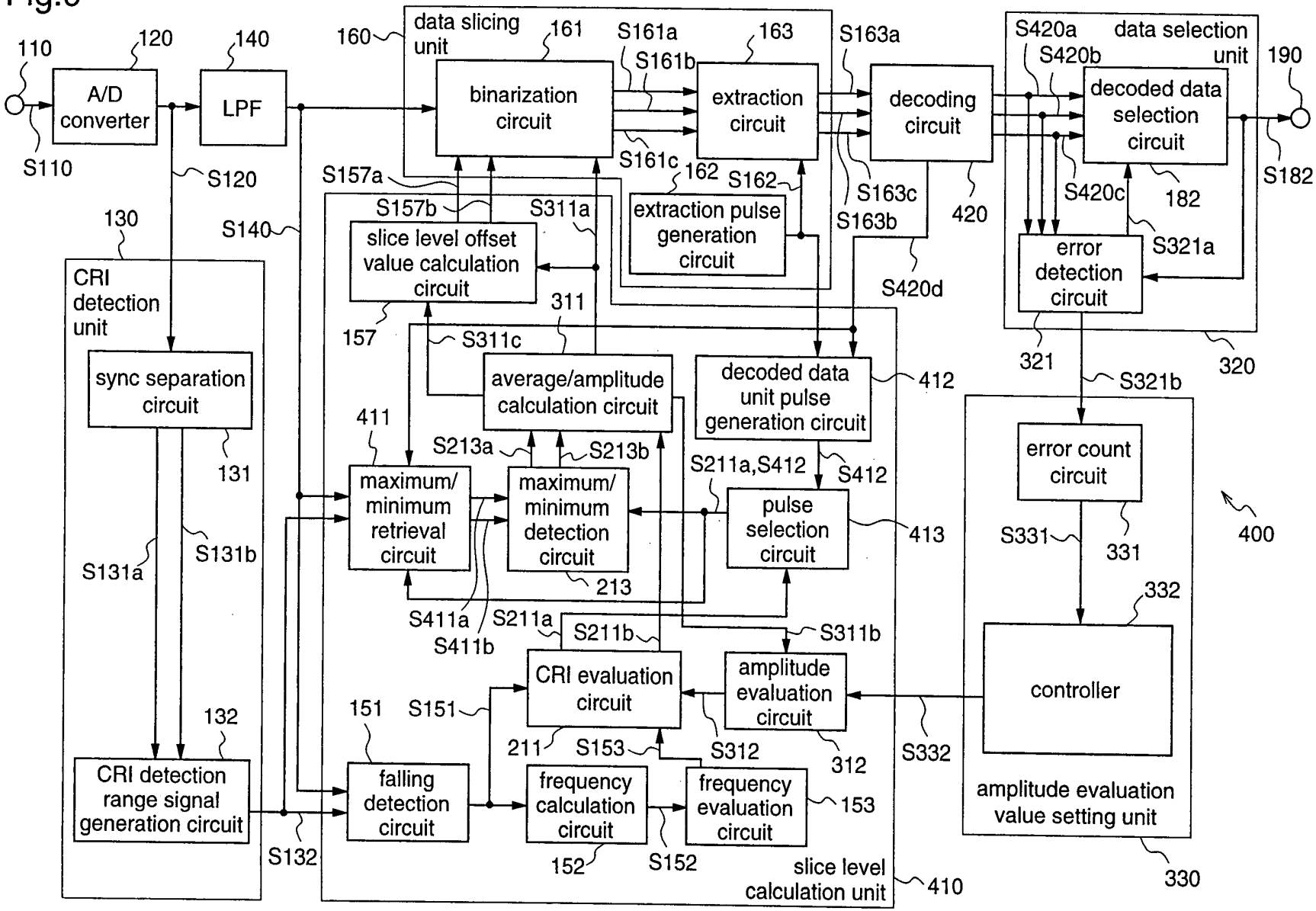
110
120
140
160
data slicing unit
161
S161a
163
S163a
S420a
data selection unit
S420b
190
A/D converter
LPF
binarization circuit
S161b
extraction circuit
decoding circuit
decoded data selection circuit
S110
S120
S161c
162
S162
S163c
S163b
420
S420c
182
S182
S157a
S157b
S311a
extraction pulse generation circuit
130
S140
slice level offset value calculation circuit
error detection circuit
S321a
CRI detection unit
311
S420d
157
S311c
321
320
sync separation circuit
average/amplitude calculation circuit
decoded data unit pulse generation circuit
412
S321b
411
S213a
S213b
S211a,S412
S412
error count circuit
131
maximum/ minimum retrieval circuit
maximum/ minimum detection circuit
pulse selection circuit
413
S331
331
400
S131a
S131b
213
332
S411a
S211a
S211b
S311b
S411b
CRI evaluation circuit
amplitude evaluation circuit
controller
151
S151
132
211
S153
S312
312
S332
CRI detection range signal generation circuit
falling detection circuit
frequency calculation circuit
frequency evaluation circuit
153
amplitude evaluation value setting unit
S132
152
S152
slice level calculation unit
410
330

Fig.10 Prior Art

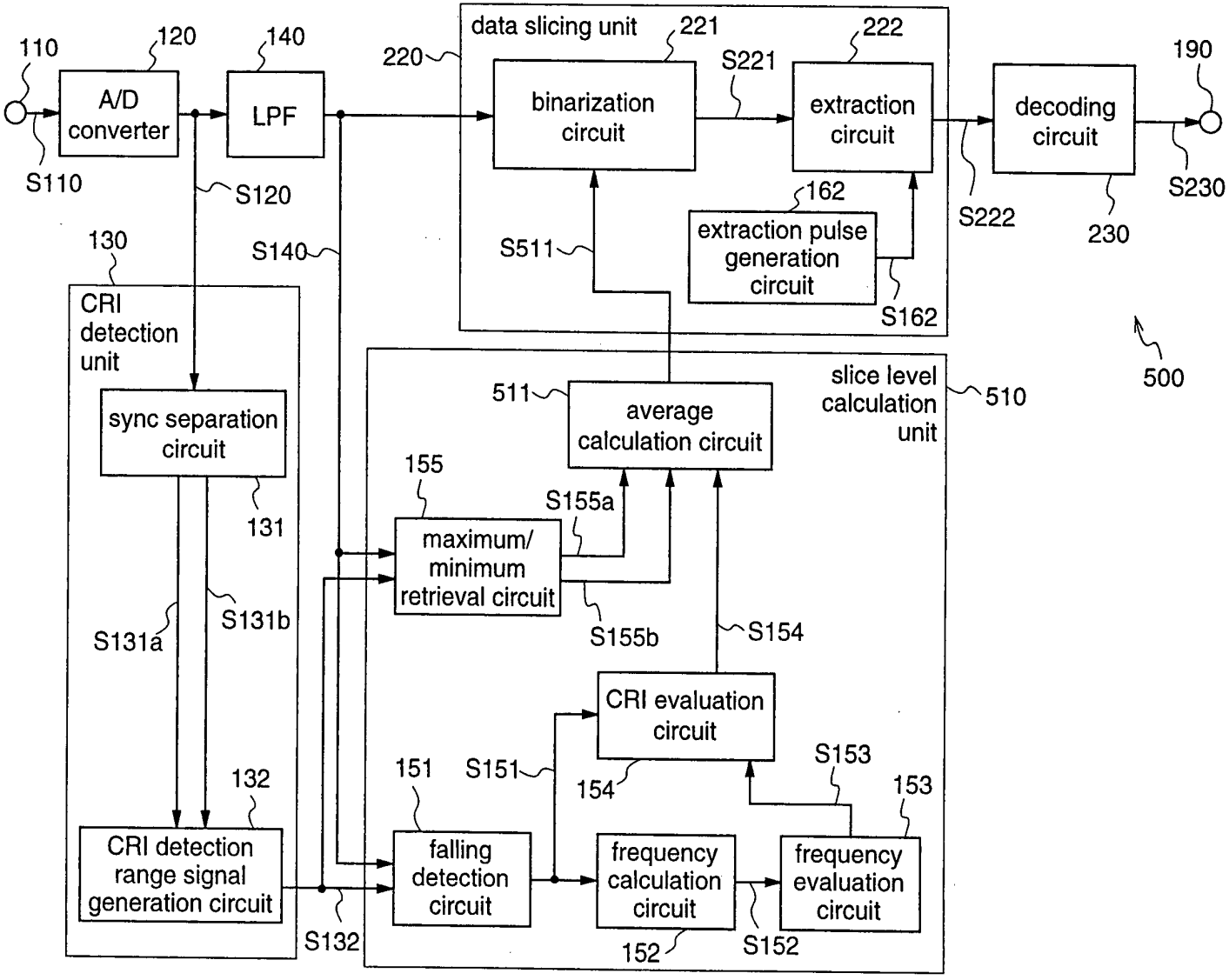

Fig.11 Prior Art

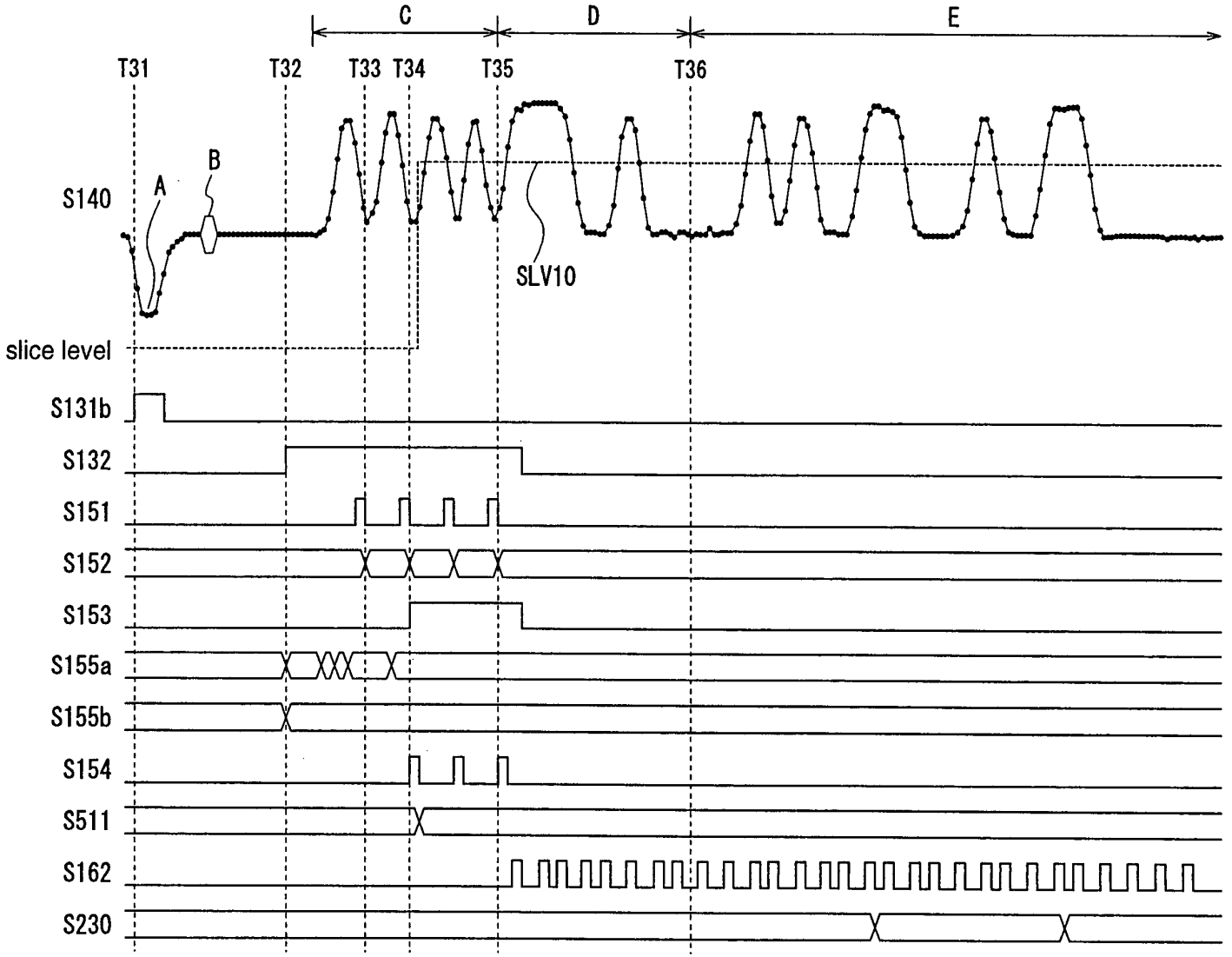
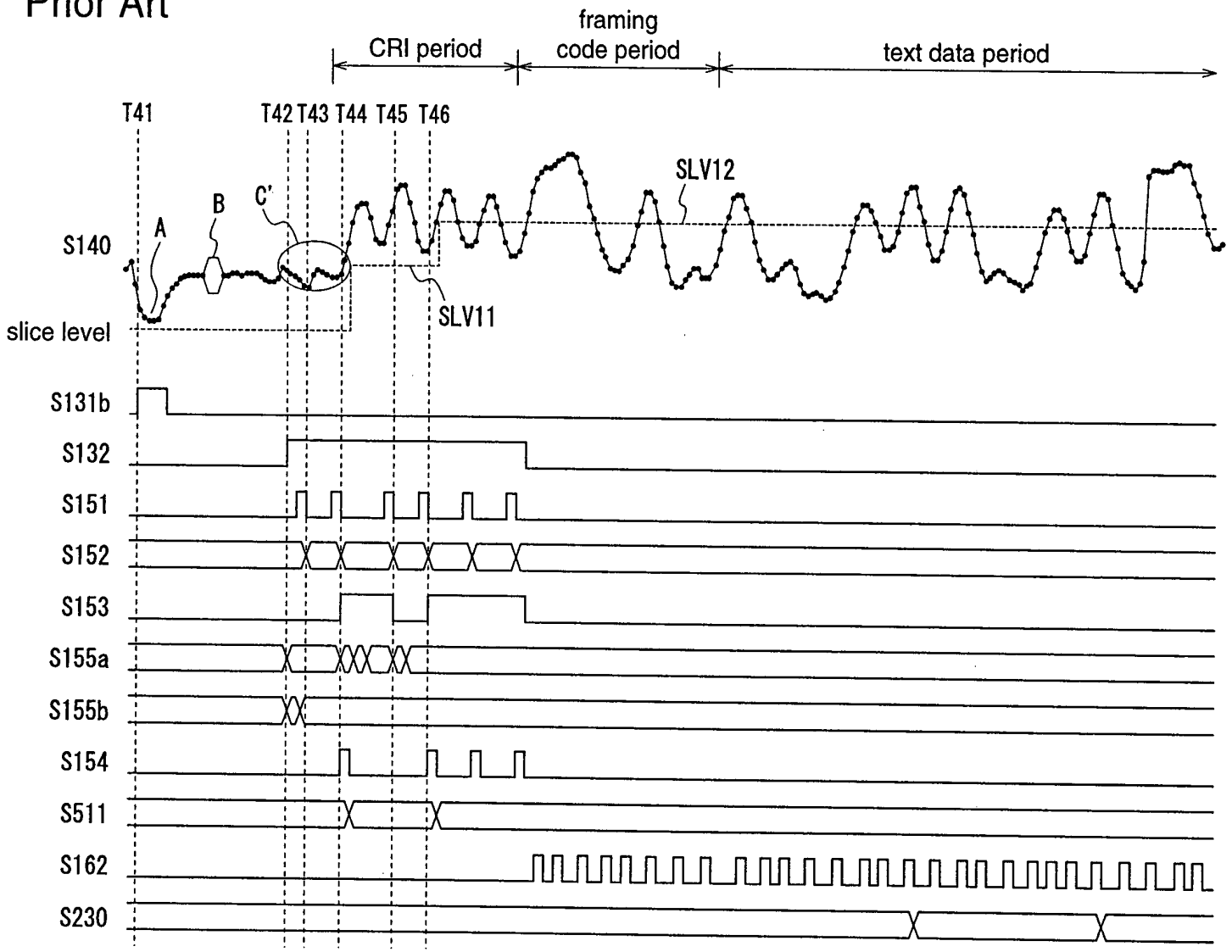
Fig.12 Prior Art